REMARKS

The application has been reviewed in light of the Office Action dated June 30, 2004. Claims 1-22 are pending, with claims 12-22 having been withdrawn by the Patent Office from consideration. By this Amendment, claims 1-11 have been amended hereby to place the claims in better form for examination, and to clarify the claimed invention. Accordingly, claims 1-11 are presented for reconsideration, with claim 1 being the sole claim in independent form which is under examination.

The title of the invention was objected to as purportedly not descriptive.

By this Amendment, the title has been amended.

Withdrawal of the objection to the title is respectfully requested.

The abstract of the disclosure was objected to as having informalities.

The abstract has been reviewed and amended to correct the formal matters noted in the Office Action.

Withdrawal of the objection to the abstract is respectfully requested.

The specification was objected to as having informalities.

The specification has been reviewed and amended to correct typographical errors and the formal matters noted in the Office Action.

A substitute specification containing the changes indicated in the Amendments To The Specification section above is attached as **Exhibit B** hereto. The substitute specification attached hereto as **Exhibit B** contains no new matter.

Withdrawal of the objection to the specification is respectfully requested.

The drawings were objected to as having informalities. The Office Action stated that proposed drawing corrections or corrected drawings for Figs. 10 and 15 are required in the reply

to the Office Action.

The replacement sheets of drawings attached hereto as **Exhibit A** include changes to, and replace, Figures 10 and 15 of the original sheets of drawings.

Withdrawal of the objection to the drawings is respectfully requested.

Claims 4 and 9 were objected to as having informalities. Claims 1-11 were rejected under 35 U.S.C. §112, second paragraph, as allegedly indefinite.

In response, the claims have been amended with particular attention to the points raised in the Office Action.

Withdrawal of the objection to the claims and withdrawal of the rejection under 35 U.S.C. §112, second paragraph, are respectfully requested.

Claim 1 was rejected under 35 U.S.C. § 102(e) as purportedly anticipated by the discussion of related art in the application. Claims 1 and 7-9 were rejected under 35 U.S.C. § 102(b) as purportedly anticipated by U.S. Patent No. 5,430,885 to Kaneko et al. Claims 2-4 were rejected under 35 U.S.C. § 103(a) as purportedly obvious over Kaneko. Claims 5, 6, 10 and 11 were rejected under 35 U.S.C. § 103(a) as purportedly obvious over Kaneko in view of Patterson et al., "Computer Architecture - A Quantitative Approach", (2nd Edition 1996).

Applicants have carefully considered the Examiner's comments and the cited art, and respectfully submit that independent claim 1 is patentable over the cited art, for at least the following reasons.

This application relates to a parallel processor and/or image processing apparatus adapted for nonlinear processing. The application describes a feature which allows assorted SIMD (single instruction stream multiple data stream) instructions to be performed.

For example, claim 1 of the present application is directed to a parallel processor comprising a global processor and a processor-element block comprising a plurality of processor elements. The global processor interprets a program and controls the entirety of the parallel processor. Each processor element comprises a register file and an operation array for processing a plurality of sets of data. Moreover, the claimed invention includes the feature that the global processor assigns to the processor elements respective processor-element numbers. The global processor can output a control signal to the processor elements, and, thereby, set the assigned processor-element numbers corresponding to the processor elements as input values of the operation arrays, respectively.

Thus, the global processor assigns the processor element numbers, and can thereby specify the number of processor elements in operation in the parallel processor. In addition, as described exemplarily in the application at page 42, lines 7-15, in an example of a SIMD processor having 128 processor elements (PE0 through PE127), the global processor can output a control signal to cause the PE numbers 0 through 127 to be loaded into the operation arrays of PE0 through PE127, respectively. With the PE numbers loaded in the respective (operation arrays of the) processor elements, many useful operations can be performed expeditiously. Some examples are described in the application at page 42, line 22 through page 54, line 3.

The background art described in the Description Of Related Art section of the application does not disclose such features. Page 11, lines 2-17 is a portion of the Summary Of The Invention section which starts at page 10, line 6. By way of contrast to summary of the invention at lines 2-8 on page 11, lines 9-13 refers to related art, in which the same value is loaded into the registers of respective PEs. For example, the related art provided for loading of the number N

into the registers of each of PE0 through PE127, which is not the feature to which the claimed invention is directed.

The other cited references likewise do not disclose or suggest the claimed invention.

Kaneko, as understood by Applicants, is directed to co-processors in a multi-processor system. Kaneko discloses that each co-processor (PE) has an inherent PE number. In one embodiment of Kaneko, the co-processors are arranged in a two-dimensional array. Therefore, a PE number in that embodiment is a pair of values (x, y). According to another embodiment of Kaneko, the co-processors are configured for three-dimensional data processing, and therefore a PE number is a triplet of values (x, y, z).

While Kaneko discloses that the co-processors, according to the configuration of the multi-processing system, have inherent PE numbers, Applicants find no teaching or suggestion in the embodiments of Kaneko, however, that the global processor assigns the processor element numbers, as provided by the claimed invention, and can thereby specify the number of processor elements in operation in the parallel processor.

Patterson is cited in the Office Action as purportedly disclosing using a general purpose register to specify a pointer, and incrementing the contents of the register after the specifying.

Applicants do not find disclosure or suggestion by the cited art, however, of a parallel processor comprising a global processor and a processor-element block comprising a plurality of processor elements, wherein the global processor assigns the processor element numbers, as provided by independent claim 1 as amended, and can thereby specify the number of processor elements in operation in the parallel processor.

Since the cited art does not disclose or suggest each and every feature of the claimed invention, the cited art does not render the claimed invention unpatentable.

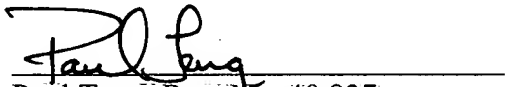
Accordingly, for at least the above-stated reasons, Applicants respectfully submit that independent claim 1, and the claims depending therefrom, are patentable over the cited art.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition. The Office is hereby authorized to charge any fees that may be required in connection with this amendment and to credit any overpayment to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Allowance of this application is respectfully requested.

Respectfully submitted,



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